Amendments to the Claims:

[c1] ~~OLE_LINK2~~1. (Currently Amended) A method of determining whether an integrated circuit operates at a clock speed, said integrated circuit comprising a combinatorial element, said method comprising:
determining a load offered by said combinatorial element when an output path of said combinatorial element switches in response to a vector provided as an input to said combinatorial element; and
performing a timing analysis of said integrated circuit by associating said load to a prior element driving said combinatorial element.

[c2] 2. (Original) The method of claim 1, further comprising:
determining another load offered by said combinatorial element when an output path of said combinatorial element does not switch in response to a vector provided as an input to said combinatorial element; and
performing another timing analysis of said integrated circuit by associating said another load to said prior element.

[c3]3. (Original) The method of claim 2, wherein said timing analysis is performed when said integrated circuit is being analyzed for hold time violations of sequential elements contained in said integrated circuit.

[c4]4. (Original) The method of claim 2, wherein said another timing analysis is performed when said integrated circuit is being analyzed for setup time violations of sequential elements contained in said integrated circuit.

[c5]5. (Currently Amended) A method of characterizing a load offered by a cell on an input pin, wherein said cell is contained in a library, said method comprising:
determining a first set of input vectors that would cause an output path of a combinatorial element to switch, wherein said combinatorial element is contained in said [[first]] cell and connected to said input pin;

measuring a capacitance of said pin when said first set of input vectors are applied to said combinatorial element; and

associating said capacitance to said pin if said cell is to be characterized for setup time violation.

[c6] 6. (Original) The method of claim 5, further comprising:
determining a second set of input vectors that would not cause said output path to switch;
measuring a capacitance of said pin when said second set of input vectors are applied to said combinatorial element; and
associating said capacitance to said pin if said cell is to be characterized for hold time violation.

[c7] 7. (Original) A machine readable medium carrying one or more sequences of instructions for causing a system to determine whether an integrated circuit operates at a clock speed, said integrated circuit comprising a combinatorial element, wherein execution of said one or more sequences of instructions by one or more processors contained in said system causes said one or more processors to perform the actions of:
determining a load offered by said combinatorial element when an output path of said combinatorial element switches in response to a vector provided as an input to said combinatorial element; and
performing a timing analysis of said integrated circuit by associating said load to a prior element driving said combinatorial element.

[c8] 8. (Original) The machine readable medium of claim 7, further comprising:
determining another load offered by said combinatorial element when an output path of said combinatorial element does not switch in response to a vector provided as an input to said combinatorial element; and
performing another timing analysis of said integrated circuit by associating said another load to said prior element.

[c9]9. (Original) The machine readable medium of claim 8, wherein said timing analysis is performed when said integrated circuit is being analyzed for hold time violations of sequential elements contained in said integrated circuit.

[c10] 10. (Original) The machine readable medium of claim 8, wherein said another timing analysis is performed when said integrated circuit is being analyzed for setup time violations of sequential elements contained in said integrated circuit.

[c11] 11. (Currently Amended) A machine readable medium carrying one or more sequences of instructions for causing a system to determine a load offered by a cell on an input pin, wherein said cell is contained in a library, wherein execution of said one or more sequences of instructions by one or more processors contained in said system causes said one or more processors to perform the actions of:
determining a first set of input vectors that would cause an output path of a combinatorial element to switch, wherein said combinatorial element is contained in said [[first]] cell and connected to said input pin;
measuring a capacitance of said pin when said first set of input vectors are applied to said combinatorial element; and
associating said capacitance to said pin if said cell is to be characterized for setup time violation.

[c12] 12. (Original) The machine readable medium of claim 11, further comprising:
determining a second set of input vectors that would not cause said output path to switch;
measuring a capacitance of said pin when said second set of input vectors are applied to said combinatorial element; and
associating said capacitance to said pin if said cell is to be characterized for hold time violation.